IN THE CLAIMS

Please cancel claims 1-218 and add the following new claims 219-245 as follows:

1-218. (Cancelled)

219. (New) A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal;

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal;

wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being offset canceled and reset in response to an HSYNC signal indicating the end of a video line.

220. (New) A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal;

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal;

wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being offset canceled and reset in response to a random time interval.

221. (New) The digitizer according to Claim 220, wherein each differential pre-amp of the array of differential pre-amps is a member of a set of pre-amp groups wherein corresponding members of each of the pre-amp groups are offset canceled and reset simultaneously.

222. (New) The digitizer according to Claim 220, wherein differential output signals from each of the array of differential pre-amps are input to a multiplexer circuit, the multiplexer circuit outputting the set of differential output signals having those differential output signals from those pre-amps in the array of differential pre-amps that are not being offset canceled and reset.

223. (New) A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal;

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal;

wherein the folding and interpolating circuit includes a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation.

224. (New) The digitizer according to Claim 223, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

225. (New) The digitizer according to Claim 224, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

226. (New) The digitizer according to Claim 224, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

227. (New) The digitizer according to Claim 226, wherein each sub-block provides four differential output signals.

228. (New) The digitizer according to Claim 224, wherein the first folding circuit includes 12 coupled sub-blocks.

229. (New) The digitizer according to Claim 223, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

230. (New) The digitizer according to Claim 229, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

231. (New) The digitizer according to Claim 230, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

232. (Original) The digitizer according to Claim 230, wherein the second folding circuit includes sixteen second folding sub-blocks.

233. (New) A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal;

wherein the comparator bank includes:

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch; and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative;

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively.

234. (New) A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal;

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal;

wherein the digital encoder includes:

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number

corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number; and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number indicating the number of the set of digitized course signals having a second logic level.

235. (New) The digitizer of Claim 234, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

236. (New) The digitizer of Claim 235, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

237. (New) The digitizer of Claim 234, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

238. (New) The digitizer of Claim 234, wherein the digital decoder further includes an error correction circuit.

239. (New) The digitizer of Claim 238, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

240. (New) The digitizer of Claim 234, wherein the digital decoder further includes a range correction circuit.

241. (New) The digitizer of Claim 240, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

242. (New) A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal;

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator

and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal;

wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

243. (New) The digitizer of Claim 242, wherein the set of differential folded signals includes 32 differential folded signals.

244. (New) The digitizer of Claim 243, wherein the set of differential course output signals includes 7 differential course output signals.

245. (New) The digitizer of Claim 244, wherein the digitized signal includes 8 bits.